Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

BEC015 - ASIC DESIGN

Sixth Semester

Course (catalog) description

An **application-specific integrated circuit** (**ASIC**) is an integrated circuit customized for a particular use, rather than intended for general-purpose use. In this course, the reader is introduced to various ASIC architectures, ASIC design flow, issues in ASIC design and testing of ASICs and also about SOC Design

Compulsory/Elective course: Elective for ECE students

Credit hours **:** 3 credits

Course Coordinator **:** Ms.M.Jasmin, Asst. Professor, Department of ECE

Instructor(s) **:**

Name of the instructor	Class handling	Office location	Office phone	Email domain: @bharathuniv.ac.in	Consultation
Ms.M.Jasmin	IV	SA 006		jasmine.ece	12.30-1.30 PM

Relationship to other courses

Pre – requiste : BEC 302- Principles of Digital Electronics and BEC 402-Electronic Circuits

Assume Knowledge : Basic knowledge in Digital System Design and Electronic circuits

Following courses : Nil

Syllabus Contents

INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN 9 HOURS

Types of ASICs - Design flow – CMOS transistors- CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors - Transistor parasitic capacitance – Logical effort - Library cell design – Library architecture.

PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9 HOURS

Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs - Xilinx I/O blocks.

PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC 09 DESIGN SOFTWARE AND LOW LEVEL DESIGN 9 HOURS

Entry: Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Low level design language - PLA tools EDIF- CFI design representation.

SILICON ON CHIP DESIGN 9 HOURS

Voice over IP SOC - Intellectual Property – SOC Design challenges- Methodology and design-FPGA to ASIC conversion – Design for integration-SOC verification-Set top box SOC.

PHYSICAL AND LOW POWER DESIGN 9 HOURS

Over view of physical design flow- tips and guideline for physical design- modern physical design techniques- power dissipation-low power design techniques and methodologies-low power design tools- tips and guideline for low power design.

Text book(s) and/or required materials

REFERENCES :

R1 M.J.S. Smith, —Application Specific Integrated Circuits , Pearson Education, 2008

R2 Wayne Wolf, —FPGA-Based System Design , Prentice Hall PTR, 2009.

R3 Farzad Nekoogar and Faranak Nekoogar, —From ASICs to SOCs: A Practical Approach , Prentice Hall PTR, 2003.

R4 www.vhdl.org/rassp/vhdl/guidelines/DesignReq.pdf

Computer usage: Nil

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area : Communication | Signal Processing | **Electronics** | **VLSI** | Embedded

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	February 2nd Week	Session 1 to 14	2 Periods
2	Cycle Test-2	March 2nd Week	Session 15 to 27	2 Periods
3	Model Test	April 3rdWeek	Session 1 to 45	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

Learn about the basic concepts for the circuit configuration for the design of linear integrated circuits and develops skill to solve engineering problems:	Correlates to program outcome		
	H	M	L
1 Recognize need for programmable devices.	a,h	c,e,f,g,i	k
2.Describe architecture of programmable devices.	c,g,j	a	b,i
3.Explain programmable methodologies.	b,k	a, c,g,h,i	-
4. Recall IC fabrication techniques vis-à-vis CMOS switch	b,c	a,e,i,k	-
5. Relate design and implementation flow for PLDs		e,f,g,k	b,i
6. low power design techniques and methodologies.	f	d,e,g	-

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture

Session	Topics	Problem Solving (Yes/No)	Text / Chapter
UNITI : INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN			
1,2	Types of ASICs & Design flow	No	R1-Chapter 1
3	CMOS transistors & CMOS Design rules	No	R1-Chapter 2
4	Combinational logic Cell	No	
5	Sequential logic cell	No	
6	Transistor as Resistors - Transistor parasitic capacitance	No	
7	Logical effort	No	
8	Library cell design	No	R1-Chapter 3
9	Library architecture.	No	
UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS			
10	Anti fuse	No	R1-Chapter 4
11	Static RAM - EPROM and EEPROM technology, PREP benchmarks	No	
12	Actel ACT	No	R1-Chapter 5
13	Altera FLEX	No	
14	Altera MAX	No	
15,16	DC & AC inputs and outputs	No	
17,18	Xilinx I/O blocks	No	R1-Chapter 6
UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY			
19	Actel ACT	No	R1-Chapter 7
20	Xilinx LCA	No	
21	Xilinx EPLD	No	
22	Altera MAX 5000 and 7000	No	
23	Altera MAX 9000, Altera FLEX	No	
24	Design systems & Logic Synthesis	No	R1-Chapter 8
25	Half gate ASIC	No	
26	Low level design language, PLA tools	No	R1-Chapter 9
27	EDIF- CFI design representation.	No	
UNITIV- SILICON ON CHIP DESIGN			
28,29	Voice over IP SOC - Intellectual Property	No	R3 –Chapter 1
30,31	SOC Design challenges- Methodology and design	No	
32	FPGA to ASIC conversion	No	R3 –Chapter 2
33	Design for integration	No	R3 –Chapter 3
34,35	SOC verification	No	
36	Set top box SOC	No	
UNIT-V- PHYSICAL AND LOW POWER DESIGN			
37	Over view of physical design flow	No	R3 Chapter 4

38	Tips and guideline for physical design	No	
39,40	modern physical design techniques	No	
41,42	power dissipation -low power design techniques and methodologies	No	R3 Chapter 5
43	low power design tools	No	
44,45	tips and guideline for low power design.	No	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures
- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	10%
Cycle Test – II	-	10%
Model Test	-	25%
Attendance	-	5%
Final exam	-	50%

Prepared by: **M.Jasmin,** Assistant Professor ,Department of ECE **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate:

a) an ability to apply knowledge of mathematics, science, and engineering fundamentals.

b) an ability to identify, formulate, and solve engineering problems

c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

d)an ability to design and conduct experiments, as well as to analyze and interpret data

e)an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

f)an ability to apply reasoning informed by a knowledge of contemporary issues

g)an ability to broaden the education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context

h) an ability in understanding of professional and ethical responsibility and apply them in engineering practices

i) an ability to function on multidisciplinary teams

j) an ability to communicate effectively with the engineering community and with society at large

k) an ability in understanding of the engineering and management principles and apply them in Project and finance management as a leader and a member in a team.

Program Educational Objectives

PEO1: PREPARATION:

To provide strong foundation in mathematical, scientific and engineering fundamentals necessary to analyze, formulate and solve engineering problems in the field of Electronics and Communication Engineering.

PEO2: CORE COMPETENCE:

To enhance the skills and experience in defining problems in Electronics and Communication Engineering design and implement, analyzing the experimental evaluations, and finally making appropriate decisions.

PEO3: PROFESSIONALISM:

To enhance their skills and embrace new Electronics and Communication Engineering Technologies through self-directed professional development and post-graduate training or education

PEO4: SKILL:

To provide training for developing soft skills such as proficiency in many languages, technical communication, verbal, logical, analytical, comprehension, team building, inter personal relationship, group discussion and leadership skill to become a better professional.

PEO5: ETHICS:

Apply the ethical and social aspects of modern communication technologies to the design, development, and usage of electronics engineering.

Course Teacher	Signature
Ms M.Jasmin	

Course Coordinator	Academic Coordinator	Professor In-Charge	HOD/ECE
(Ms..Jasmin)	( )	( )	(Dr M.Sundararajan)